REMARKS

Claims 13, 14, 32-37, 40-45, and 48-53 are amended, and claims 56-60 are added; as a result, claims 13-16 and 32-60 are now pending in this application. Reconsideration of the application is respectfully requested.

The term "buffer" is amended to "first" in claim 13, 14, 32-36, 40-45, and 48-53. These amendments are not made for purposes of patentability as discussed in *Festo v. Shoketsu Kinzoku Kogyo Kabushiki Co.* 72 F.3d 558 (Fed. Cir. 2000). Accordingly, these elements are entitled to a full scope of equivalents.

Reservation of the Right to Swear Behind References

Applicant maintains its right to swear behind any references which are cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

§103 Rejection of the Claims

Claims 36-39 are rejected under 35 USC § 103(a) as being unpatentable over Katayama et al. (U.S. 5,875,452). Applicant respectfully traverses.

Applicant respectfully notes that Katayama does not teach or suggest all of elements recited in claim 36. For example, Figures 1 and 9 of Katayama do not show "a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder; ...a command buffer ...and a data buffer [emphasis added]." The Office Action states that "the plurality of sense amps 28 (note column 17, lines 12-14) in Figure 2 would have required multiple dedicated read and write buffers 54 and 52." However, the undersigned can find no reference at column 17, lines 12-14 of such a teaching as contained in the claims. Specifically, it is believed that Katayama does not teach a plurality of memory devices having a data in and data out buffer, column decoder and row decoder. Applicant respectfully requests further clarification as to where this teaching is found in Katayama.

Moreover, if Katayama's read and write buffers are read as the data in and the data out buffer as recited in claim 36, then Katayama does not have a data buffer that is connected to a

plurality of memory devices. Katayama's Figure 2 clearly demonstrates the same, wherein data in and data out buffer 52, 54 are only connected to one memory device and the data I/O bus. Katayama's Figure 9 merely shows a single buffer 78 connected to the plurality of memory devices 22 and bus 18. Claim 36 recites, in part, two buffers, namely, a data in and a data out buffer and a data register. Accordingly, Katayama does not teach all of the elements of claim 36; and claim 36 patentably distinguishes over Katayama under 35 U.S.C. §103.

The Office Action further relies on St. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977) for not lending patentable weight to each of the memory devices having a data in and a data out buffer. Applicant cannot agree with this assertion. Specifically, the feature of each memory device containing a data in and a data out buffer, a column decoder and a row decoder was added to claim 36 to clarify that these components are in each memory device and that within the memory system an address register and a data register corresponding to a plurality of memory devices are in addition to the internal components of each memory device because these features do, in fact, lend patentable weight. For example, the corresponding address register and data register result in an effect greater than the sum of the several effects taken separately. For example and as illustrated in Figure 1 of the present application memory system 100 comprises N command and address buffers 131, N data buffers and N*M DRAMS. Each command and address buffer drives the latched command and address information to its corresponding plurality of memory devices. In this manner, the load on the C/A bus is reduced from N*M devices to only N devices. Additionally, the load on data bus 120 is reduced from N*M devices to only N devices. As a result the effects of the data in and data out buffer of each of the plurality of memory devices, in combination with the address register and the data register within the memory system are more than the sum of the single effects of the internal components of each of the plurality of memory devices. The addition of an address register coupled between a corresponding plurality of memory devices and a unidirectional command and address bus and a data register coupled between the corresponding plurality of memory devices and a bidirectional data bus results in a memory system which uses a single 16-bit data bus which can be operated at 800 MHZ and which supports 64 devices. In sum, the present invention as defined by the claims is not obvious under §103. And is certainly not analogous to the courts resolution in St. Regis interpretation of redundancy which found merely adding layers to a paper bag as in was obvious.

It should further be noted that the office action admits that Katayama et al. does not specifically mention the connector as recited in claim 36. The Office Action asserts that the use of sockets in data processing systems was well known at the time of the invention. Applicant respectfully traverses this assertion as a form of official notice and requests a reference to support the assertion or withdrawal of the assertion according to MPEP 2144.03.

Moreover, applicant submits that claim 36 is patentable over Katayama et al. based at least on the fact that Katayama et al. does not teach a connector and the registers as recited in claim 36. Claims 37-39 depend from claim 36 are allowable at least because they depend from claim 36. Withdrawal of the §103 rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 21 day of December, 2001.

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Docket No. 303.306US4 Micron Ref. No. 96-0214.03
WD # 402381

CLEAN VERSION OF PENDING CLAIMS

PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS
Applicant: Kevin J. Ryan
Serial No.: 09/434,654

Claims 13-16 and 32-60, as of December 21, 2001 (Date of Response to First Office Action).

13. (Amended) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a memory module, wherein the memory module includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a second, data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the

unidirectional command and address bus and to the bidirectional data bus.

14. (Amended) The memory system according to claim 13 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

15. The memory system according to claim 13 wherein each memory device is a dynamic random access memory device.

16. The memory system according to claim 13 wherein M equals 8.

32. (Amended) A method of storing data in a pipelined memory system, wherein the pipelined memory system includes a memory module, a socket, and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder, and a row decoder, and wherein the socket couples the memory module to a unidirectional command and address bus and to a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

communicating data, through the socket to the memory module, on the bidirectional data bus;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

33. (Amended) The method of claim 32, wherein communicating commands and addresses and communicating data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

34. (Amended) A method of reading data in a pipelined memory system, wherein the pipelined memory system includes a memory module and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the socket to a memory controller, on the bidirectional data bus.

35. (Amended) The method of claim 34, wherein communicating commands and addresses and receiving data includes executing a packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

36. (Amended) A memory module comprising:

a data register;

a first register;

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, and further contains a column decoder and a row decoder, wherein the data in buffer receives data information from the data register and wherein the column decoder and row decoder receive address information from the first register; and

a connector, wherein the connector includes command and address lines coupled to the first register and data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

37. (Amended) The memory module of claim 36, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

38. The memory module of claim 36, wherein each memory device is a dynamic random access memory device.

39. The memory module of claim 36, wherein M equals 8.

40. (Amended) A method of storing data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

receiving data, through the data lines, from the data bus;

latching the commands and addresses in the first register;

latching the data in a data register;

driving the latched commands and addresses to a plurality of memory devices having

addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

41. (Amended) The method of claim 40, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

42. (Amended) A method of reading data in a memory module having a connector, wherein the connector includes command and address lines coupled to a first register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

reading data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the data lines, to the data bus.

43. (Amended) The method of claim 42, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

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44. (Amended) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a memory module, wherein the memory module includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

45. (Amended) The electronic system of claim 44, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the first register of the memory module and a second delay introduced by the data register of the memory module.

plurality of memory devices, wherein each memory device includes the same, wherein

46. The electronic system of claim 44, wherein each memory device is a dynamic random access memory device.

47. The electronic system of claim 44, wherein M equals 8.

48. (Amended) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of storing data in one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address bus;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

communicating data from the memory controller to the bidirectional data bus;

communicating the data from the bidirectional data bus to the memory module;

latching the commands and addresses in a first register;

latching the data in a data register;

driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

49. (Amended) The method of claim 48, wherein communicating commands and addresses and communicating data includes executing a pipeline packet protocol which incorporates a first

delay introduced by the first register and a second delay introduced by the data register.

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50. (Amended) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of reading data from one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

latching the commands and addresses in a first register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the socket to the memory controller, on a bidirectional data bus.

51. (Amended) The method of claim 50, wherein communicating commands and addresses and receiving data includes executing a pipeline packet protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

52. (Amended) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device;

a memory module, wherein the memory module includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a first register connected between the command and address bus and the plurality of memory devices, the first register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

53. (Amended) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the data register.

54. The memory system of claim 52, wherein each memory device is a dynamic random access memory device.

55. The memory system of claim 52, wherein M equals 8.

56. (New) A memory module having a plurality of pipelined memory subsystems, wherein each pipelined memory subsystem includes:

a first register;

a second register;

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder, and a row decoder, wherein the data in buffer receives data information from the first register and wherein the column decoder and row decoder receive address information from the second register; and

a connector, wherein the connector includes command and address lines coupled to the second register and data lines coupled to the first register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

57. (New) The memory module of claim 56, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the first register and a second delay introduced by the second register.

58. (New) The memory module of claim 56, wherein each memory device is a dynamic random access memory device.

59. (New) The memory module of claim 56, wherein M equals 8 and the number of memory subsystems equals two.

60. (New) The memory module of claim 56, wherein M equals 8 and the number of memory subsystems equals one.